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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/544,801 | 04/07/2000 | Shunpei Yamazaki | SEL 174 | 1717 |

7590 03/26/2007

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| EXAMINER | |
|---|---|
| ERDEM, FAZLI | |
| **ART UNIT** | **PAPER NUMBER** |
| 2826 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/26/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/544,801 | YAMAZAKI ET AL. | |
| | Examiner | Art Unit | |
| | Fazli Erdem | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-14,17-23,26,27,68-71 and 76-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14,17-23,26, 27, 84 and 85* is/are allowed.

6)☒ Claim(s) *68-71,76-83 and 86-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### Examiner's Comment

1. Applicant is reminded that references 6,593,592 and 6,569,717 are included in the Form 892 because the examiner believes these references are also related to the Yamazaki reference that is used to make the 35 USC 102 rejection below.

### *Allowable Subject Matter*

1. Claims 10-14, 17-23, 26, 27, 84 and 85 allowed.

2. The following is a statement of reasons for the indication of allowable subject matter: Prior art failed to establish a pixel TFT and a driver TFT, driver TFT comprising a first n-channel TFT and a second n-channel TFT, wherein the gate electrode of said pixel TFT and a gate electrode of said driver TFT comprise a first conductive layer, and wherein said gate electrodes of pixel TFT and driver TFT are in electrical contact with gate wirings comprising a second conductive layer areas outside channel forming of said pixel TFT and said driver TFT.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 68-71, 76-83, 86-88 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 68-71, 76-83, 86-88 independent claims 68, 76 and 80 disclose "a storage capacitor comprising a portion of said semiconductor layer, a portion of said gate insulating film, a same material as said first conductive layer and a same material as said second conductive layer." In these claims it is not clear and indefinite if the word "same" is referring to the gate insulating film or the semiconductor layer.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 68-71 and 76-88 rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (6,573,564).

Regarding Claims 68-71, examiner takes the position that, there is a capacitance formed when an insulating/dielectric layer is sandwiched between two conductive layers and hence a transistor is in itself could be thought of a transistor since a gate insulating layer is sandwiched between a gate electrode and a channel region.

Regarding Claim 68, in Fig. 2C, 6B, 10A, 14C, 15 and in claims 23, 31 and 35, Yamazaki et al. disclose a semiconductor device and fabrication method thereof where a semiconductor layer 112 over a substrate said semiconductor layer comprising a pair of impurity regions and a channel forming region interposed between, a gate electrode 103 and a gate4 insulating film 102, gate wiring 1510 in contact with gate electrode, and a storage capacitor comprising a portion of the semiconductor layer 112, gate insulating layer 102, gate wiring 1510 and gate electrode 117.

Regarding Claim 69 gate electrode is formed of aluminum or tantalum as shown in column 11, lines 55-65.

Regarding Claim 70, in figs. 2C, 6B, 10A, 14C and 15, Yamazaki et al. disclose an electroluminescent device.

Regarding Claim 71 Figs 24A-24F disclose the required display device selected from personal computer, video camera or digital camera.

Regarding Claim 86, Yamazaki et al. disclose active matrix liquid crystal display device.

Regarding Claim 76, in Fig. 2C, 6B, 10A, 14C, 15 and in claims 23, 31 and 35, Yamazaki et al. disclose a semiconductor device and fabrication method thereof where a semiconductor layer 112 over a substrate said semiconductor layer comprising a pair of impurity regions and a channel forming region interposed between, a gate electrode 103 and a gate4 insulating film 102, gate wiring 1510 overlapping gate electrode, gate wiring formed outside channel forming regions and a storage capacitor comprising a portion of

the semiconductor layer 112, gate insulating layer 102, gate wiring 1510 and gate electrode 117.

Regarding Claim 77 gate electrode is formed of aluminum or tantalum as shown in column 11, lines 55-65

Regarding Claim 78, in figs. 2C, 6B, 10A, 14C and 15, Yamazaki et al. disclose an electroluminescent device.

Regarding Claim 79 Figs 24A-24F disclose the required display device selected from personal computer, video camera or digital camera.

Regarding Claim 87, Yamazaki et al. disclose active matrix liquid crystal display device.

Regarding Claim 80, in Fig. 2C, 6B, 10A, 14C, 15 and in claims 23, 31 and 35, Yamazaki et al. disclose a semiconductor device and fabrication method thereof where a semiconductor layer 112 over a substrate said semiconductor layer comprising a pair of impurity regions and a channel forming region interposed between, a gate electrode 103 and a gate4 insulating film 102, gate wiring 1510 in contact with gate electrode, gate wiring formed outside channel forming regions and a storage capacitor comprising a portion of the semiconductor layer 112, gate insulating layer 102, gate wiring 1510 and gate electrode 117.

Regarding Claim 81 gate electrode is formed of aluminum or tantalum as shown in column 11, lines 55-65

Regarding Claim 82, in figs. 2C, 6B, 10A, 14C and 15, Yamazaki et al. disclose an electroluminescent device.

Regarding Claim 83 Figs 24A-24F disclose the required display device selected from personal computer, video camera or digital camera.

Regarding Claim 88, Yamazaki et al. disclose active matrix liquid crystal display device.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
March 13, 2007

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER